an encapsulant made of the molding compound for encapsulating the chip, the buffer pad, the heat sink and the chip carrier, wherein the interface layer and the side surfaces of the heat sink are exposed to outside of the encapsulant, the side surfaces of the heat sink are flush with side edges of the encapsulant, and the molding compound left on the interface layer during formation of the encapsulant is easily removable from the interface layer, so as to make the semiconductor package free of flash of the molding compound because of the relatively smaller adhesion between the interface layer and the molding compound.

REMARKS

Claims 1-20 are pending in the application. Claims 1 and 12 have been amended by the present amendment. The amendments are fully supported by the specification as originally filed.

The drawings were objected to under 37 CFR 1.83(a) for failing to show "an encapsulant made of the molding compound for encapsulating the chip, the buffer pad, the heat sink and the chip carrier," as recited in claims 1 and 12. As shown in FIGS. 2(E) to 2(H), encapsulant 24 encapsulates the chip 21, the heat sink 23, and the chip carrier 20 (see also page 8, second paragraph of specification). Upon removing layer 240A of the encapsulant, as shown in FIG. 2(H), the fabricated semiconductor package of FIG. 1 is produced (or FIG. 4, according to another embodiment). With reference to FIG. 4, a buffer pad 48 can be attached to chip 41 and heat sink 43, which are encapsulated by an encapsulant 44 (see also page 10, first full paragraph). Therefore, the above-cited limitations of claims 1 and 12 are clearly shown in the drawings and fully described in the accompanying specification. It is respectfully requested that the drawing objections be withdrawn.

The present invention is directed to a semiconductor package with a heat sink, in which the heat sink is dimensioned to maximize an exposed surface thereof, so as to prevent resin flash and improve heat-dissipating efficiency (see specification at page 3, first full paragraph). As recited in claims 1 and 12, the heat sink includes a first surface and a second surface opposed to the first surface, wherein the first surface is directly attached to a chip (claim 1) or attached to a

buffer pad (claim 12) interposed between the heat sink and the chip. An interface layer is formed on the second surface of the heat sink, and made of a material having adhesion with a molding compound **smaller** than adhesion between the heat sink and the molding compound.

The semiconductor package of the Applicants' invention can be implemented with the heat sink being attached to the chip in a batch-type manner, as shown in FIGS. 2(A) to 2(H), thereby simplifying the fabrication process and reducing its cost. Moreover, the interface layer formed on the second surface of the heat sink provides adhesion between the interface layer and the molding compound which is **smaller** than that between the first surface of the heat sink and the molding compound. The interface layer preferably is made of a metallic material having poor adhesion to the molding compound, e.g., gold, chromium, nickel, alloys thereof, or Teflon, which therefore does not undesirably affect heat dissipation through the heat sink.

FIG. 2(H) illustrates the semiconductor package after encapsulation with a molding compound (reference numerals 24 and 240A). Because adhesion between interface layer 233 and molding compound 240A is **smaller** than adhesion between heat sink 23 and molding compound 24, the molding compound 240A left on the interface layer 233 can be easily removed, without leaving resin flash on the interface layer 233, such that the resulting semiconductor package is free of resin flash (see FIG. 1), thus improving the heat-dissipating efficiency of the semiconductor package.

Claims 1-4, 6, 9, and 10 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 6,288,900 to Johnson et al. (hereinafter "Johnson") in view of U.S. Patent 4,848,646 to Morishita et al. (hereinafter "Morishita"). Claim 5 was rejected under 35 USC 103(a) as being unpatentable over Johnson and Morishita, and further in view of U.S. Patent 6,127,724 to DiStefano. Claims 7 and 8 were rejected under 35 USC 103(a) as being unpatentable over Johnson and Morishita, and further in view of U.S. Patent 6,198,171 to Huang et al. Claim 11 was rejected under 35 USC 103(a) as being unpatentable over Johnson and Morishita, and further in view of U.S. Patent 6,323,065 to Karnezos. Claims 12-16, 19, and 20 were rejected under 35 USC 103(a) as being unpatentable over Johnson and Morishita, and further in view of

U.S. Patent 6,236,568 to Lai et al. Claims 17 and 18 were rejected under 35 USC 103(a) as being unpatentable over Johnson and Morishita, and further in view of Lai et al., and further in view of Huang et al. These rejections are respectfully traversed.

Johnson is directed to a flip-chip, ball grid array (BGA) package, and specifically addresses the problem of mismatched coefficients of thermal expansion (CTE) between the material comprising the chip and the organic laminate material (see column 1, lines 11-17), which causes the package to warp and leads to fatigue failure. In order to prevent warpage of the package, Johnson teaches a package with a heat spreading cap that is "shaped or sized to provide distinct combinations of stiffness and CTE in at least two areas" (column 2, lines 30-32).

With reference to FIGS. 15 and 16 of Johnson, as cited in the Office Action, heat spreading cap 22 comprises "two different layers 40 and 41" (column 4, line 65; FIG. 15), or "three different layers" (column 5, line 4), i.e., two layers 41 which sandwich one layer 40 (FIG. 16). In Johnson, the heat spreading cap is attached to the chip by means of an encapsulant "which is usually an epoxy" (see column 3, lines 36-38), which corresponds to encapsulant 24 in FIGS. 15 and 16.

Johnson fails to teach or suggest an **interface layer** as recited in the Applicants' claimed invention (see claims 1 and 12). Johnson does not teach or suggest any equivalent to the claimed interface layer, which maximizes the exposed surface area for heat dissipation and prevents resin flash. Johnson also fails to teach or suggest an interface layer or equivalent thereof which is "made of a material having adhesion with a molding compound smaller than adhesion between the heat sink and the molding compound," as required in claims 1 and 12.

Johnson actually teaches away from the Applicants' claimed invention because, as shown in FIGS. 15 and 16, the heat spreading cap 22 is adhered to encapsulant (i.e., an epoxy resin) 24, which has poor thermal properties as known to anyone of ordinary skill in the art. In contrast, the Applicants' claimed invention requires that the heat sink be directly attached to a chip and/or buffer pad, in order to effectively dissipate heat from the package.

It should be pointed out that reference numeral 41 in Johnson does not correspond to the claimed "interface layer," as cited in the Office Action. Johnson clearly teaches that the layer 41 is one layer of the heat spreading cap 22 (see column 4, lines 64-65). As admitted on page 4 of the Office Action, Johnson does not disclose "a material ... and a size of the interface layer" – it is apparent that Johnson does not teach or suggest an interface layer at all – the layer 41 is merely one layer of the heat spreading cap 22. Layer 41 cannot be considered an "interface layer" as recited in claims 1 and 12 and explained in the specification.

Morishita fails to remedy the deficiencies of the Johnson reference. Morishita is directed to a method for depositing solder onto aluminum metal material, which addresses difficulties in the prior art of joining solder to aluminum (see column 1, lines 7-10). The method of Morishita is applicable only to aluminum processing, and involves steps of substituting zinc on the activated surface of the aluminum and forming a nickel coating film on the zinc-substituted surface by a non-electrode plating method. This method is applied specifically at the spot where soldering is to be performed, so the zinc-substituted layer and the nickel coating film are not exposed on portions of the metal material which do not require soldering, and for preventing electrolytic corrosion due to potential gradient with aluminum (see column 3, lines 44-52). In other words, Morishita teaches a method of soldering a metal onto aluminum, in order to increase the bonding or adhesion between the soldering metal and the aluminum.

With reference to FIG. 2 of Morishita, as cited in the Office Action, heat sink 10 is plated with the zinc-substituted layer 11, which is covered with the nickel coating film 12. The nickel coating film 12 is provided for the purpose of improving soldering between the metals so as to increase adhesion therebetween, whereas the nickel coating film allows the usual soldering onto the aluminum metal. Morishita fails to teach or suggest an **adhesion layer** as recited in claims 1 and 12 of the Applicants' claimed invention. Morishita also does not teach or suggest that the coating film 12 has "adhesion with a molding compound smaller than adhesion between a heat sink and a molding compound" – therefore, the coating film 12 is not equivalent to the claimed "adhesion layer." Moreover, Morishita specifically teaches that the coating film 12 is strongly adhered to soldering material 3, which teaches away from the Applicants' claimed invention.

As stated in column 4, lines 10-13 of Morishita: "When a semiconductor element was soldered onto the thus formed nickel coating film, the soldering material was rigidly and readily adhered to the nickel coating film."

Therefore, Morishita does not teach or suggest an "interface layer" as claimed, and according to Morishita, the nickel coating film 12 must be strongly adhered to soldering material 3, which teaches away from the Applicants' claimed invention. Therefore, even if Morishita were somehow combined with Johnson, the Applicants' claimed invention could not be produced. There would be no teaching or suggestion of the claimed "interface layer" or an equivalent having the features recited in claims 1 and 12, for at least the reasons discussed above.

With reference to the rejection of claim 12, FIG. 2 of Lai teaches a buffer pad 5 which is disposed between a chip 3 and a heat-conductive piece 4. However, for at least the reasons discussed above, Lai cannot be added to the combination of Johnson in view of Morishita to produce the Applicants' invention as recited in claim 12.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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APPENDIX A:
VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 1 and 12 have been amended as follows:

1. (Amended) A semiconductor package with a heat sink, comprising:

a chip carrier;

at least one chip mounted on the chip carrier and electrically connected to the chip carrier;

a heat sink having a first surface, a second surface opposed to the first surface, and a plurality of side surfaces interconnecting the first surface and the second surface, wherein the first surface of the heat sink is attached to the chip for interposing the chip between the chip carrier and the heat sink;

an interface layer formed on the second surface of the heat sink, and made of a material having adhesion with a molding compound smaller than adhesion between the heat sink and the molding compound, wherein the interface layer covers the entire second surface of the heat sink; and

an encapsulant made of the molding compound for encapsulating the chip, the heat sink and the chip carrier, wherein the interface layer and the side surfaces of the heat sink are exposed to outside of the encapsulant, [and] the side surfaces of the heat sink are flush with side edges of the encapsulant, and the molding compound left on the interface layer during formation of the encapsulant is easily removable from the interface layer, so as to make the semiconductor package free of flash of the molding compound because of the relatively smaller adhesion between the interface layer and the molding compound[;

whereby due to relatively smaller adhesion between the interface layer and the molding compound for making the encapsulant, the molding compound remaining on the interface layer during formation of the encapsulant can be removed easily from the interface layer, so as to make the semiconductor package free of flash of the molding compound].

12. (Amended) A semiconductor package with a heat sink, comprising:

a chip carrier;

at least one chip mounted on the chip carrier and electrically connected to the chip carrier;

at least one buffer pad attached to the chip and made of a material having a similar thermal expansion coefficient to the chip;

a heat sink having a first surface, a second surface opposed to the first surface, and a plurality of side surfaces interconnecting the first surface and the second surface, wherein the first surface of the heat sink is attached to the buffer pad for interposing the buffer pad between the heat sink and the chip so as to space the first surface apart from the chip;

an interface layer formed on the second surface of the heat sink, and made of a material having adhesion with a molding compound smaller than adhesion between the heat sink and the molding compound, wherein the interface layer covers the entire second surface of the heat sink; and

an encapsulant made of the molding compound for encapsulating the chip, the buffer pad, the heat sink and the chip carrier, wherein the interface layer and the side surfaces of the heat sink are exposed to outside of the encapsulant, [and] the side surfaces of the heat sink are flush with side edges of the encapsulant, and the molding compound left on the interface layer during formation of the encapsulant is easily removable from the interface layer, so as to make the semiconductor package free of flash of the molding compound because of the relatively smaller adhesion between the interface layer and the molding compound[;

whereby due to relatively smaller adhesion between the interface layer and the molding compound for making the encapsulant, the molding compound remaining on the interface layer during formation of the encapsulant can be removed easily from the interface layer, so as to make the semiconductor package free of flash of the molding compound].